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Synopsysdesigncompilercrack

December 9, 2563 BC - RTL compiler - Synopsys Design compiler. Once you have modeled and verified that your Verilog code is working correctly, you can compile. The RTL compiler was designed to be a powerful tool for chip programming, and this is one of the reasons why it works so well. While C and C++ compilers can support different architectures and instruction sets at the same time, Verilog compilers only support the i8051 architecture. The RTL compiler was designed with the expectation that it would be used primarily for programming chips for applications requiring a high level of abstraction.



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